ALPHA DATA

XRM2-ADC-D6/250 User Manual

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1 Introduction

Figure 1 : XRM2-ADC-D6/250

The XRM2-ADC-D6-250 is a front panel adapter card designed for use with Alpha Data's FPGA cards using Virtex 6 and later FPGAs.

The XRM2-ADC-D6-250 provides two dc-coupled channels of analogue to digital conversion with 14 bit resolution and supports sampling rates up to 250 MHz . It is aimed at applications such as IF/Baseband Signal Sampling.

A companion card, the XRM2-ADC-D6-250-AC, uses the same ADC architecture but employs a wideband transformer to drive the ADC thus maintaining dynamic performance over a wider bandwidth.

An external clock source may be used or an internally generated clock can be used to provide the sampling clock.

Two auxiliary I/O ports are provided for use as trigger inputs and general purpose signalling. A further pair of ports are provided for inter-board connection, fast triggering etc.

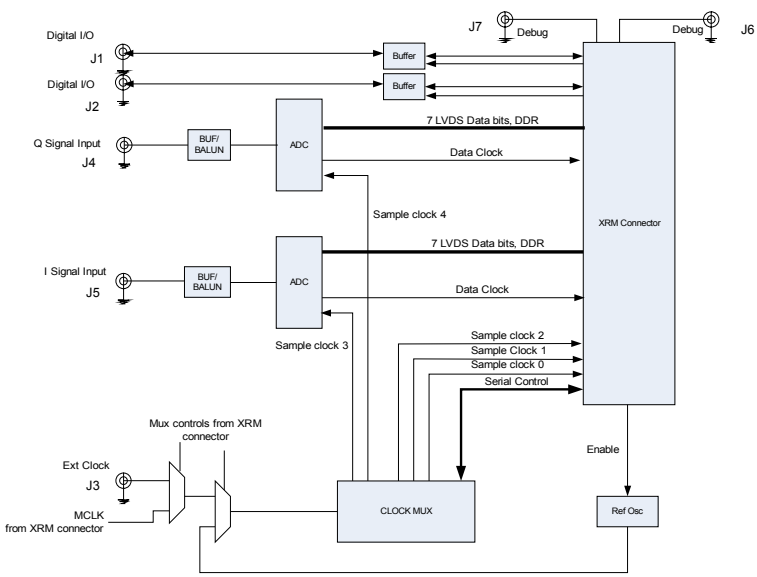

Figure 2 : XRM Block Diagram

Where differences between the AC performance and the DC-coupled performance exist, these are explicitly stated. If no such qualification is given then the parameter applies to both versions.

2 Installation

The XRM2-ADC-D6/250 is designed to plug in to the front panel connector (SAMTEC QSH series) on the range of Alpha Data FPGA cards indicated above. The retaining screws should be tightened to secure the XRM.

Note:
This operation should not be performed while the FPGA card is powered up.

2.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe SSD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

Avoid flexing the board.

3 Specification

3.1 Inputs

3.1.1 I Signal (J5), Q Signal (J4)

Input:	50 Ohms
Bandwidth (DC version):	DC to 450 MHz (1dB typ)
Bandwidth (AC version):	4.5 MHz to 1000 MHz (3 dB)
Level:	+12 dBm (2.5 Vppk =ADC full scale)

3.1.2 Clock In (J3)

Input:	50 Ohms, ac coupled
Level:	0 dBm (630 mV pk to pk) to +12 dBm (2.5V pk to pk) nominal

3.2 Input /Output

3.2.1 Trig IO Port (J1)

User configurable as input or output

Input:	4k7 Ohms, dc coupled
Level:	+3V3 LVTTL or +5V TTL[1]

3.2.2 Aux IO Port (J2)

User configurable as input or output

Input:	4k7 Ohms, dc coupled
Level:	+3V3 LVTTL

[1] - factory/user selectable

4 Options

4.1 Connector type

- SMA (7 mm, standard)
- Long Barrel SMA (20 mm)
- SMB
- SMC

4.2 Order Code

XRM-ADC-D6-250 -[Connector option] -[IO voltage option]

XRM-ADC-D6-250-AC -[Connector option] -[IO voltage option]

Fields in square brackets may be omitted in order to obtain the standard configuration for that option.

5 Related Documents

TBD

6 Design Examples

Example UCF, HDL files and Application software are available from Alpha Data for purchasers of this card.

Note:
This product requires an export licences for companies outwith EU, Australia, Canada, Japan, New Zealand, Norway, Switzerland or the USA. Contact the factory for further information.

7 Pinouts

Pinout information required

Analogue data is encoded in 2's complement format, with 0x1FFF (+8191) representing positive full scale and 0x2000 (-8192) representing negative full scale.

OVERRANGE goes high when the signal input is outwith the valid ADC input range.

8 Board Layout

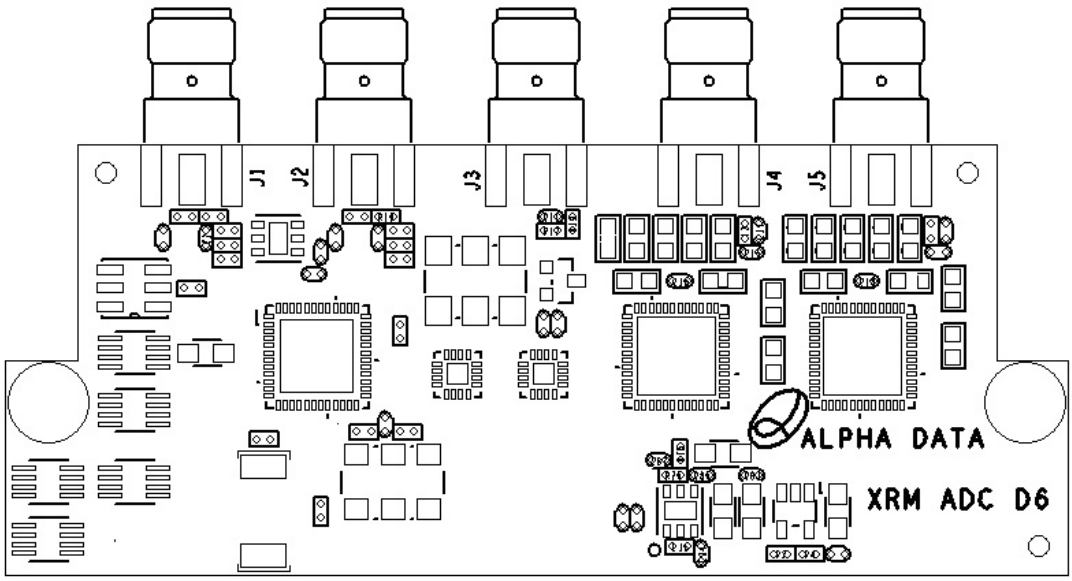

Figure 3 : XRM2-ADC-D6/250 Board Layout

Note:
This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference if not installed and used with adequate EMI protection for specific applications.

Revision History

Date	Revision	Nature of Change
July 2008	1.0	First issue
Feb 2010	1.1	Corrected minor typos
May 2010	1.2	Corrected typo regarding full scale code values.
Feb 2012	1.3	Converted to new document system
Feb 2016	1.4	Created XRM2 Version

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